Adaptive Traffic Control System for Lane Reduction

Digital Logic & Circuits Lab
Fall 2024 – 2025
Section – H | Group - 1
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Contents

Introduction

- Optimize Traffic Flow Efficiency.
- Facilitating the merging process of multiple lanes.
- Incorporation of essential features like:
    1. Clock Pulse Generator.
    2. Controllable pulse duration module.

Objectives

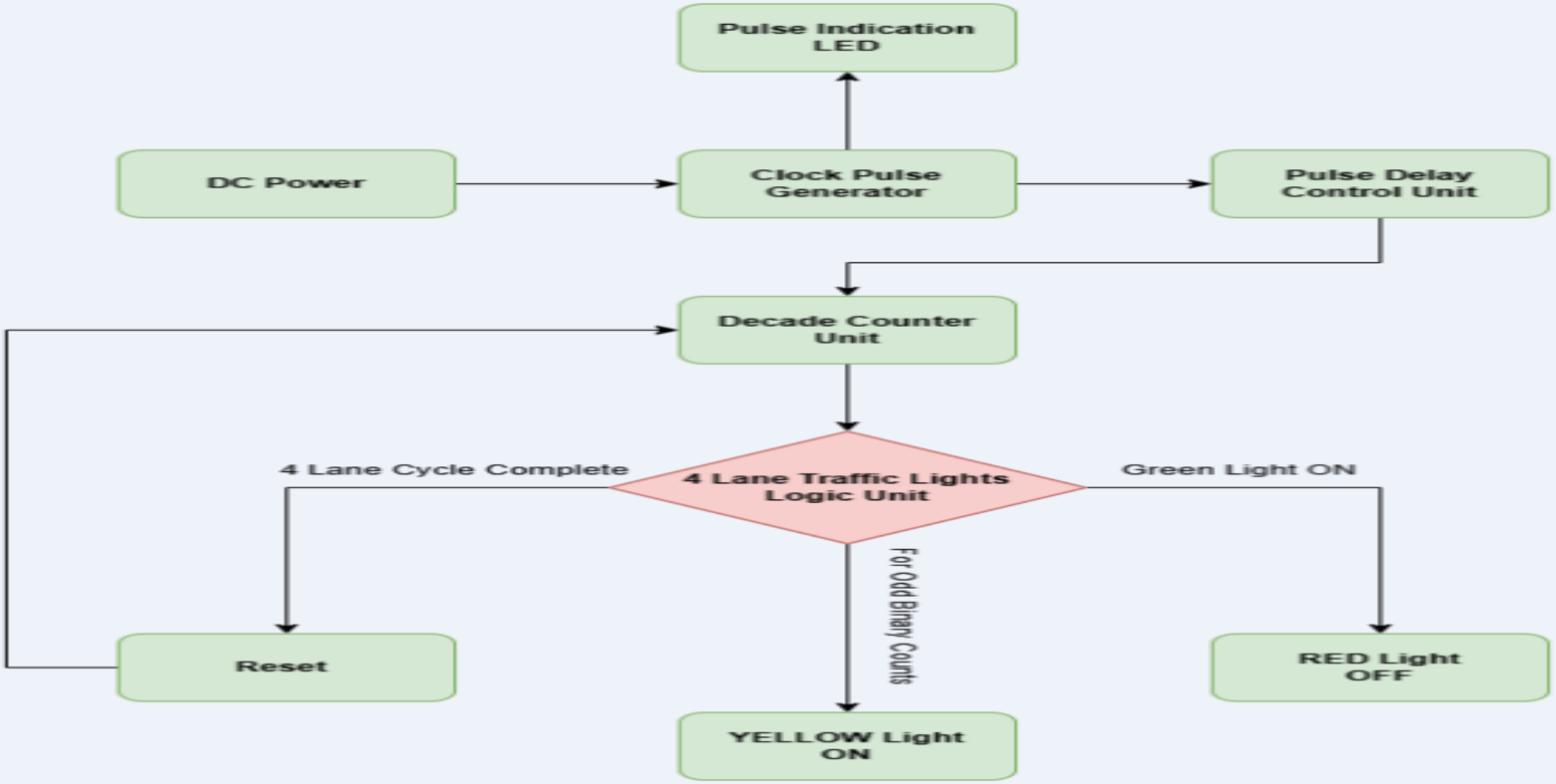
- **-The objective of the project was to -**

- Design & implement a traffic control circuit for lane reduction purpose
- Achieve reliable performance
- Ensure simplicity & ease of implementation

Motivation

- An innovative, reliable, and adaptive traffic control system is crucial for modern transportation.
- Reduction of congestion and delays caused by lane reduction scenarios.
- Significant impact of timely traffic management , extending beyond mere vehicular movement to improved urban mobility.
- Primary goal: Ensuring smoother and more efficient transportation for the public.

Block Diagram



Methodology

- The 5 stages of the Traffic Control circuit-

- Generating clock pulse using 555 timer IC
- Setting up clock pulse duration control module
- Designing a decade counter
- Implementing a 4 to 1 lane traffic light logic unit
- Setting recycle parameters

555 Timer in astable mode

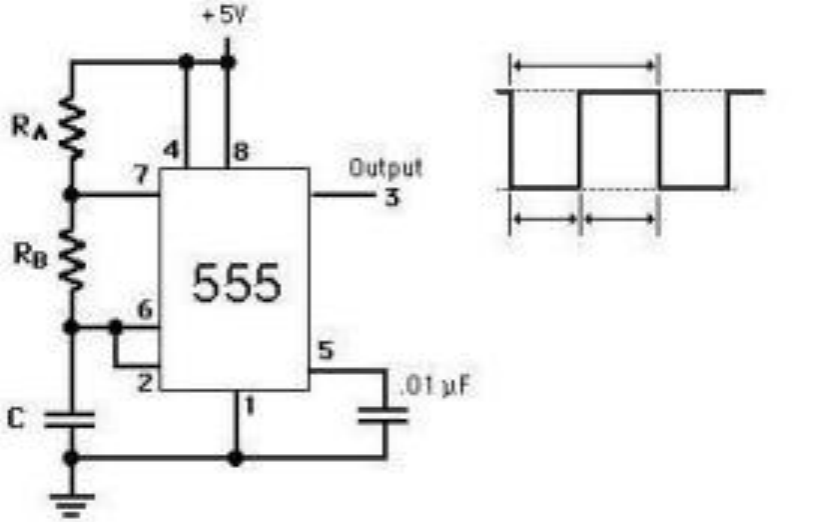


Figure-2: 555 timer connected as an astable multivibrator

- The 555 Timer is set up in Astable Mode

- It generates a continuous stream of rectangular off-on pulses that switch between two voltage levels. The frequency of the pulses and their duty cycle are dependent upon the RC network values.

Custom clock pulse duration & decade counter

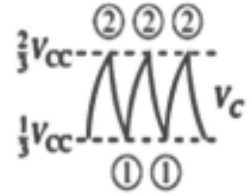


Figure-3: Charging-Discharging of Capacitor of a 555 Timer in Astable Mode

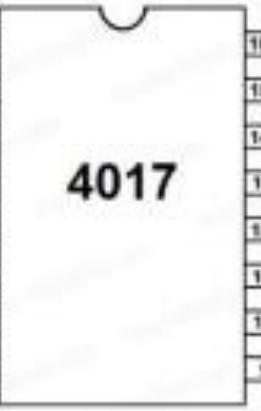


Figure-4: Decade Counter IC-4017

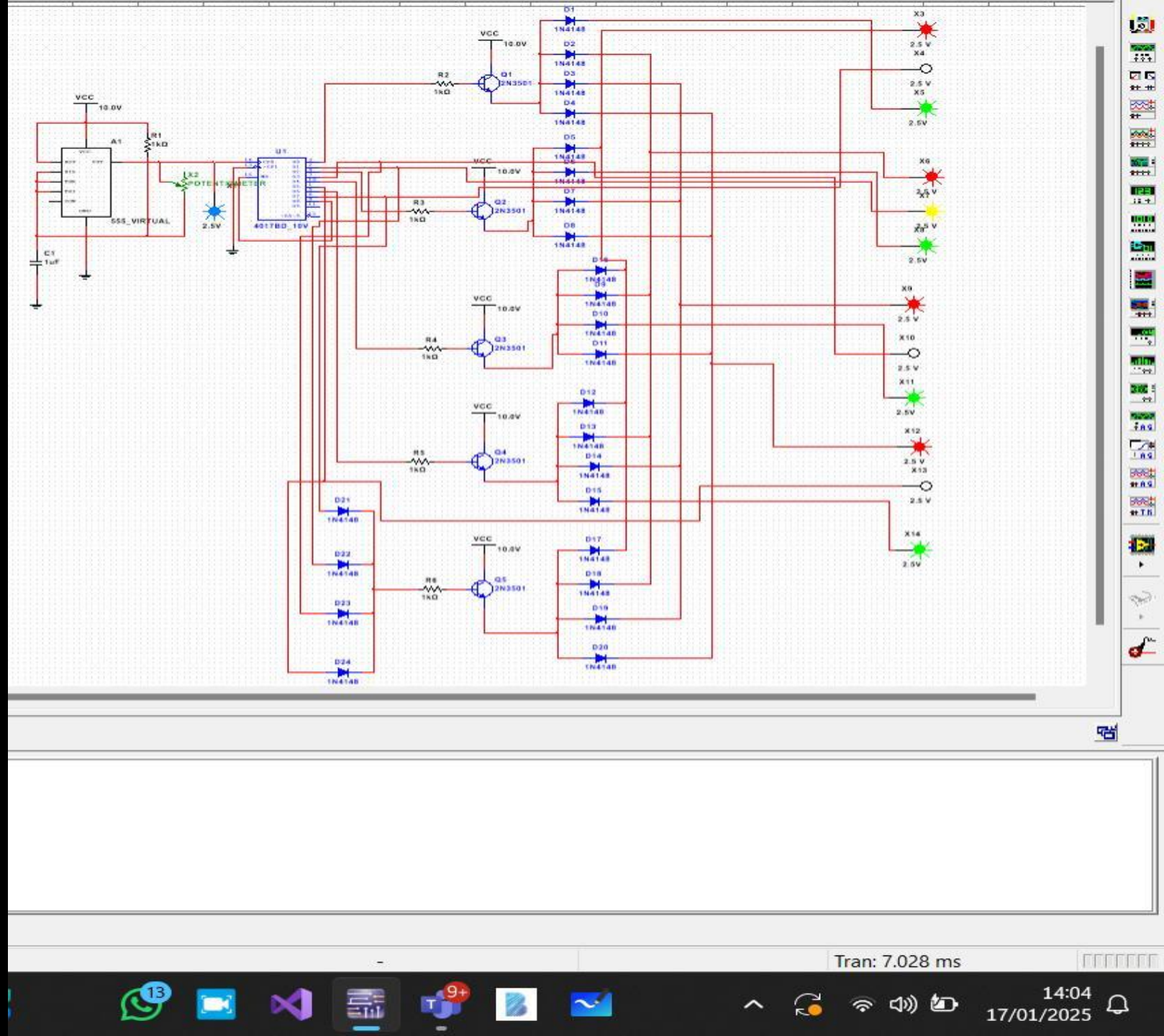
- **Custom Clock Pulse Duration:**

  A potentiometer replaced RB to regulate capacitor charging. Increased resistance lengthened capacitor charge time, extending clock pulse duration. Decreased resistance hastened capacitor charging, shortening clock pulse duration.

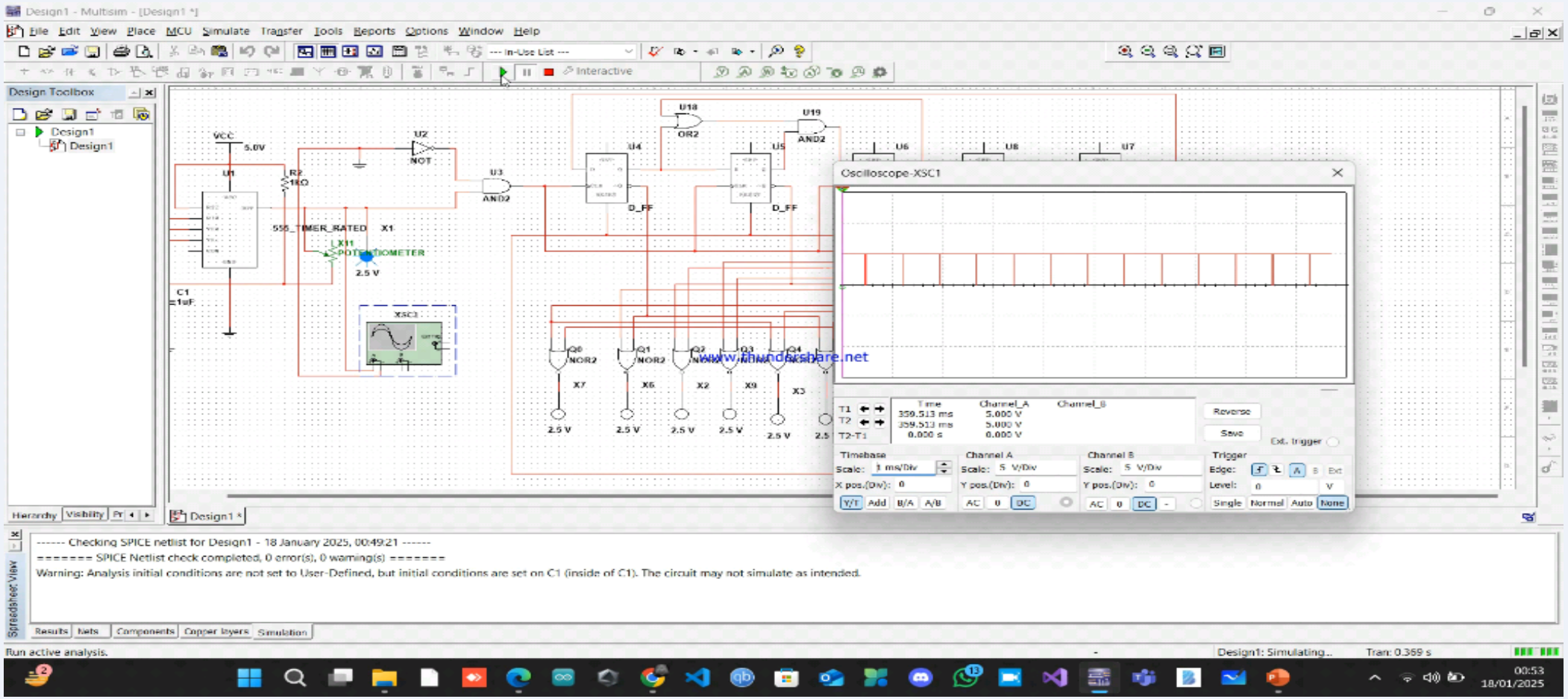
- **Decade Counter (4017 IC):**

  The 4017 IC, commonly known as a decade counter, was utilized. It is a 16-pin counter and divider chip capable of counting from 0 to 9, making it suitable for sequential output applications.

Circuit Diagram



Simulation



555 Timer in Astable mode connected to a decade counter module

Result & Discussion

- The Results -

- 555 timer in astable mode, produced stable and accurate timing signals.
- The pulse duration was adjustable using a potentiometer (POT).
- The decade counter effectively cycled through the four lanes in sequence.

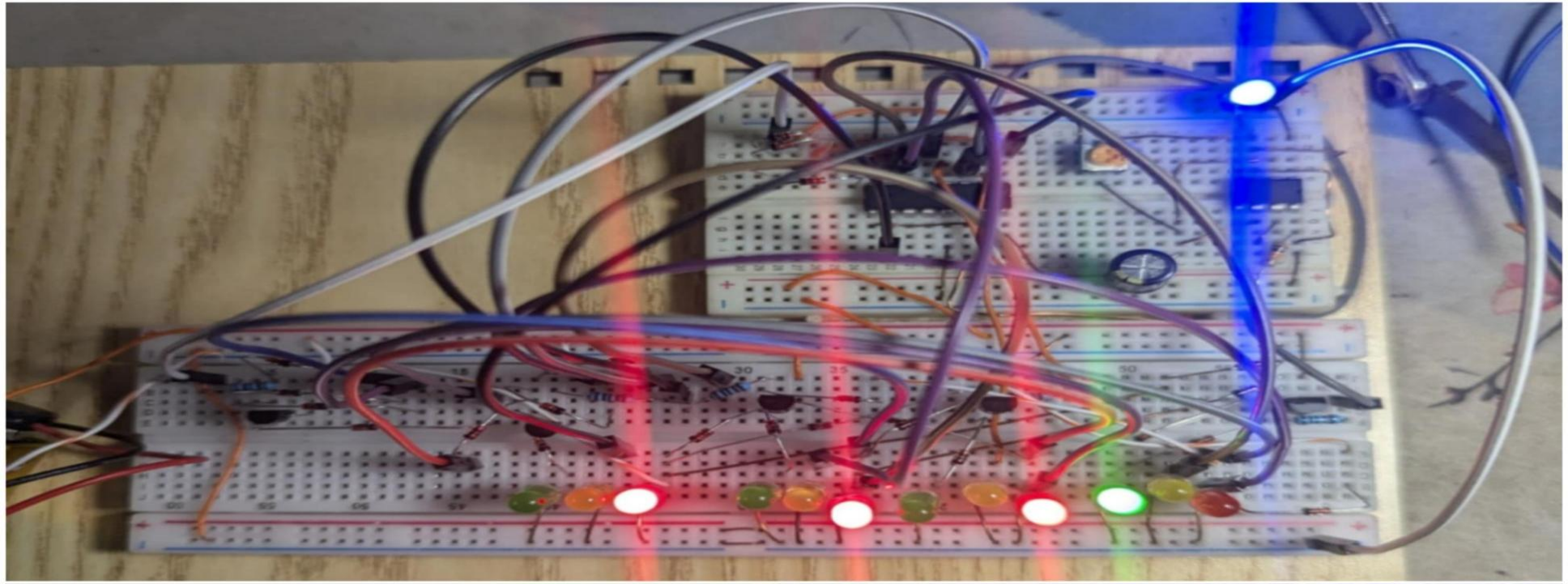
Limitations of the circuit

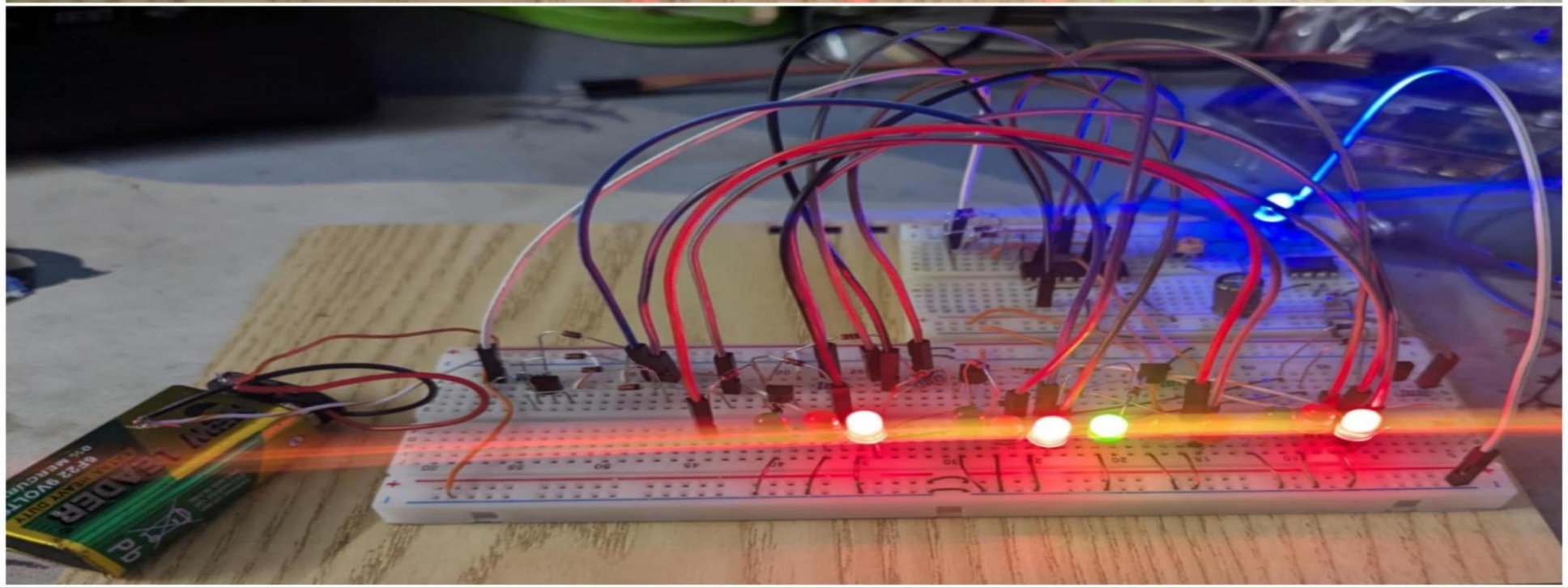
- Absence of Vehicle Detection
- Simplified Traffic Control Logic
- Reliance on Simulated Traffic Scenarios
- Limited Communication with Vehicles

Major Contribution

- Development of an adaptive traffic control system tailored for efficient lane reductions.
- Integration of dynamic signal control to minimize congestion during peak hours
- Simulation-based validation of the system's effectiveness under diverse traffic conditions.
- Proposal of a scalable framework for future urban traffic management systems.

Project Prototype





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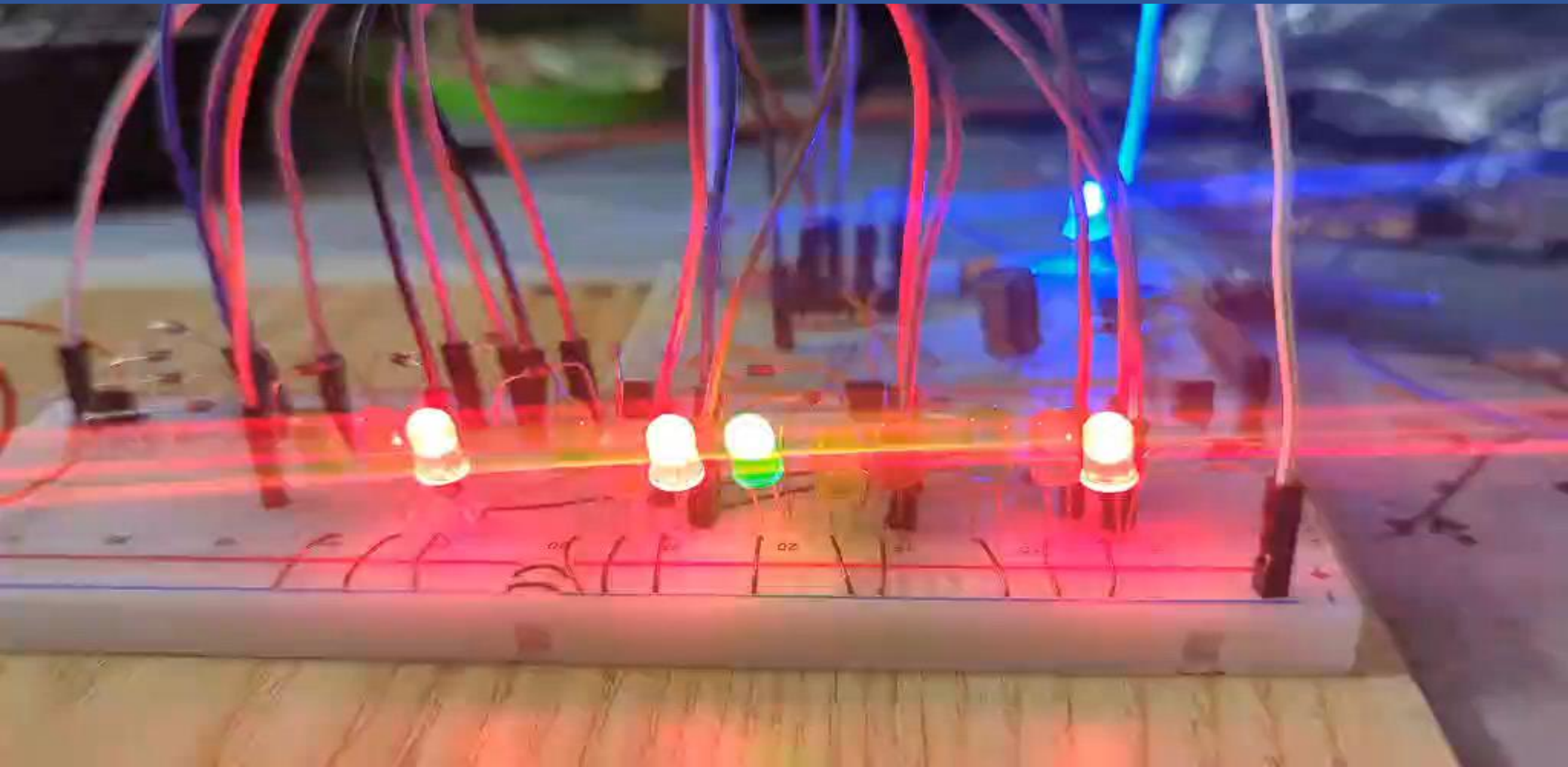

Conclusion

In conclusion, the development and testing of the Adaptive Traffic Control System for lane reduction have yielded promising results. Through the integration of critical components such as-

- the clock pulse generator
- pulse duration controller
- traffic control logic unit

The system successfully managed traffic flow during lane reduction scenarios. The circuit's reliability is further strengthened by the consistency between simulation and experimental findings.

Scope of Future Works

- Enhancement of traffic signal logic for complex scenarios
- Vehicle detection mechanism can be introduced
- Introduction of queue-length detection sensors
- Reduction of system power consumption through optimized components.

References

[1] Z. Liang, W. Gu, Y. Yang, and Y. Wang, “FPGA-based Logic Circuit Design and Implementation for Smart City Traffic Control Lights,” Aug. 2023, doi: https://doi.org/10.1109/icsece58870.2023.10263447

[2] R. Gokul, A. J. Nirmal, K. R. Bharath, M. P. Pranesh, and R. Karthika, “A Comparative Study between State-of-the-Art Object Detectors for Traffic Light Detection,” *2020 International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE)*, Feb. 2020, doi: https://doi.org/10.1109/ic-etite47903.2020.449.

[3] D. Mahanta, “Automatic Traffic Light Control System,” 2017, https://doi.org/10.13140/RG.2.2.26742.34882

[4] V. Panchal, "Four-Way Traffic Light Controller Designing with VHDL," Research Gate, 2018. doi: https://doi.org/10.13140/RG.2.1.4194.7282

[5] J. E. Ortiz and R. H. Klenke, "Simple traffic light controller: A digital systems design project," Proceedings of the IEEE SoutheastCon 2010 (SoutheastCon), Concord, NC, 2010, pp. 85-88, doi: https://doi.org/10.1109/SECON.2010.5453915

Thank You!

Special Thanks To – MD. ALOMGIR KABIR , Sir

For supervising the project. His constructive feedback have contributed significantly to the success of this project.